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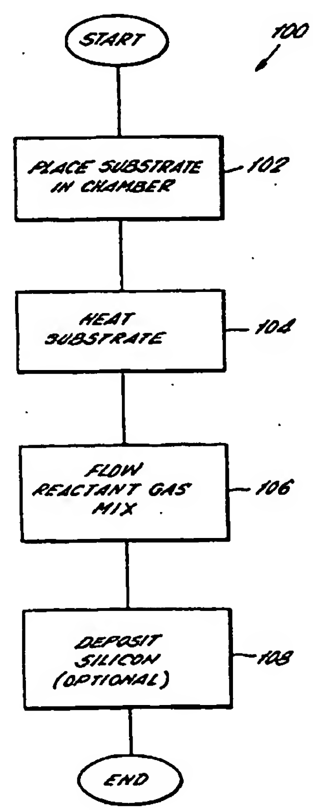
(54) Apparatus and method for surface finishing a silicon film

(57) A method of smoothing a silicon surface formed on a substrate. According to the present invention a substrate having a silicon surface is placed into a chamber and heated to a temperature of between 1000° - 1300°C. While the substrate is heated to a temperature between 1000° - 1300°C, the silicon surface is exposed to a gas mix comprising H_2 and HCl in the chamber to smooth the silicon surface.

FIG. 1



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Description

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

[0001] The present invention relates to the field of semiconductor processing and more specifically to a method and apparatus for smoothing a silicon or silicon alloy surface.

2. DISCUSSION OF RELATED ART

[0002] Semiconductor devices such as microprocessors and memories are fabricated by various steps including the deposition and removal of silicon films. Silicon deposition and removal steps as well as other process steps can cause the surface of silicon films to become rough and contaminated. Rough and contaminated silicon surfaces can generally lead to poor quality interfaces which can lead to poor device performance and reliability. It would therefore be desirable to be able to accurately, reliably, and uniformly treat a silicon surface in order to remove any surface contaminants contained therein and to provide a smooth silicon surface finish. It would also be desirable to be able to treat a silicon surface in a chamber which could subsequently be used to deposit a silicon film. In this way after removing the surface contaminants and smoothing the silicon surface one could directly deposit a silicon film onto the uncontaminated smooth silicon surface without exposing the treated surface to an oxidizing or contaminating environment.

SUMMARY OF THE INVENTION

[0003] A method of treating of a silicon surface. According to the present invention a substrate having a silicon or silicon alloy surface is placed into a chamber and heated to a temperature of between 1000° - 1300°C. While the substrate is heated to a temperature of between 1000°- 1300°C, the silicon surface is exposed to a hydrogen containing gas mix comprising H_2 and HCl in the chamber to treat the silicon surface.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] **Figure 1** is a flow chart showing a method of treating a silicon film in accordance with the present invention.

[0005] **Figure 2A** is an illustration of a processing an apparatus which can be utilized to treat a silicon film in accordance with the present invention.

[0006] **Figure 2B** is a plane view showing how a gas manifold can be divided to enable the formation of different process gas flows for different zones of the wafer.

[0007] **Figure 2C** is an illustration of a system control program which can be used to control the processes and apparatus of Figure 2A.

[0008] **Figure 3A** is an illustration of a cross-sectional view of a substrate having an outer silicon with a rough surface.

[0009] **Figure 3B** is an illustration of a cross-sectional view showing a surface treatment of the silicon film on the substrate of Figure 3A.

[0010] **Figure 3C** is an illustration of a cross-sectional view showing the formation of a silicon film on the surface treated silicon film of the Figure of 3B.

[0011] **Figure 4** is a plot which shows how silicon etch rate varies for different $HCl:H_2$ concentration ratios.

[0012] **Figure 5** is an illustration of a cluster tool which can be used to form a silicon on insulator (SOI) substrate in accordance with a implant and cleave process in accordance with the present invention.

[0013] **Figure 6A** is an illustration of a handle wafer and a donor wafer.

[0014] **Figure 6B** is an illustration showing the ion implantation of hydrogen into the donor wafer to form a dislocation therein.

[0015] **Figure 6C** is an illustration showing the plasma activation of the donor and handle wafer.

[0016] **Figure 6D** is an illustration showing the bonding of the donor wafer to the handle wafer.

[0017] **Figure 6E** is an illustration showing the cleaving of a portion of the donor wafer from the handle wafer.

[0018] **Figure 6F** is an illustration showing the treating of the top surface of the silicon film formed on the handle wafer.

[0019] **Figure 6G** is an illustration showing the formation of a silicon film on the treated silicon surface of the substrate of Figure 6F.

[0020] **Figure 6H** is an illustration showing the surface treating of the donor wafer.

[0021] **Figure 6I** is an illustration showing the formation of a silicon film on the treated silicon surface of the donor wafer.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0022] The present invention describes a method and apparatus for treating or finishing a silicon surface. In the following description numerous specific details are set forth in order to provide a through understanding of the present invention. One skilled in the art will appreciate that these specific details are not necessary in order to practice the present invention. In other instances, well known equipment features and processes have not been set forth in detail in order to not unnecessarily obscure the present invention.

[0023] The present invention is a method and apparatus for finishing or treating a silicon or silicon alloy, by smoothing the surface and removing contaminants contained therein. According to the present invention a substrate having a silicon surface is placed into a deposition chamber and heated to a temperature between 1000°

to 1300°C. While the substrate is heated, the silicon surface is exposed to a gas mix comprising hydrogen (H_2) and hydrochloric acid (HCl). The relatively high temperature used during the surface treatment is sufficient to increase silicon mobility and thereby cause silicon in high areas or peaks to migrate to low areas or valleys in the film. Simultaneously with the silicon migration the gas mix removes the top of the silicon surface resulting in a smoothing of the silicon surface and removal of contaminants contained therein. The present invention is able to smooth a silicon or silicon alloy surface with a surface roughness of 6nm RMS or more into a surface with a surface roughness of less than 0.1nm RMS. In an embodiment of the present invention the silicon surface is treated in a silicon deposition chamber so that after the silicon surface has been sufficiently smoothened, additional silicon can be added to provide a silicon layer with any desired thickness. In an embodiment of the present invention the silicon treating process is integrated into a H_2 cleave process used to form a silicon on insulator (SOI) substrate.

[0024] Figure 1 is a flow chart 100 which depicts a method of finishing or treating a silicon or silicon alloy surface in accordance with the present invention. Figure 2A is an illustration of a thermal processing apparatus 210 in which the method of the present invention can be implemented. An example of such an apparatus is the Applied Materials single wafer atmospheric "EPI" tool known as the "EPI Centura".

Apparatus For Smoothing A Silicon or Silicon Alloy Film

[0025] The processing apparatus 210 shown in Figure 2A, is a deposition reactor and comprises a deposition chamber 212 having an upper dome 214, a lower dome 216 and a sidewall 218 between the upper and lower domes 214 and 216. Cooling fluid (not shown) is circulated through sidewall 218 in order to cool "o" rings used to attach domes 214 and 216 to sidewall 218. An upper liner 282 and a lower liner 284 are mounted against the inside surface of sidewall 218. The upper and lower domes 214 and 216 are made of a transparent material to allow heating light to pass through into the chamber 212.

[0026] Within the chamber 212 is a flat, circular susceptor 220 for supporting a wafer in a horizontal position. The susceptor 220 extends transversely across the chamber 212 at the sidewall 218 to divide the chamber 212 into an upper portion 222 above the susceptor 220 and a lower portion 224 below the susceptor 220. The susceptor 220 is mounted on a shaft 226 which extends perpendicularly downwardly from the center of the bottom of the susceptor 220. The shaft 226 is connected to a motor (not shown) which rotates shaft 226 and thereby rotates the susceptor 220. An annular preheat ring 228 is connected at its outer periphery to the inside periphery of lower liner 284 and extends around the susceptor 220. The preheat ring 228 is in the same plane as the susceptor 228 with the inner edge of the pre-heat ring 228 separated by a gap 229 from the outer edge of the susceptor 220.

[0027] An inlet manifold 230 is positioned in the side of chamber 212 and is adapted to admit gas from a source of gas or gases, such as tanks 140, into the chamber 212. An outlet port 232 is positioned in the side of chamber 212 diagonally opposite the inlet manifold and is adapted to exhaust gases from the deposition chamber 212.

[0028] A plurality of high intensity lamps 234 are mounted around the chamber 212 and direct their light through the upper and lower domes 214 and 216 onto the susceptor 220 (and preheat ring 222) to heat the susceptor 220 (and preheat ring 222). Susceptor 220 and preheat ring 222 are made of a material, such as silicon carbide, coated graphite which is opaque to the radiation emitted from lamps 234 so that they can be heated by radiation from lamps 234. The upper and lower domes 214 and 216 are made of a material which is transparent to the light from the lamps 234, such as dear quartz. The upper and lower domes 214 and 216 are generally made of quartz because quartz is transparent to light of both visible and IR frequencies; it exhibits a relatively high structural strength; and it is chemically stable in the process environment of the deposition chamber 212. Although lamps are the preferred means for heating wafers in deposition chamber 220, other methods may be used such as resistance heaters and RF inductive heaters. An infrared temperature sensor 236 such as a pyrometer is mounted below the lower dome 216 and faces the bottom surface of the susceptor 220 through the lower dome 216. The temperature sensor 236, is used to monitor the temperature of the susceptor 220 by receiving infra-red radiation emitted from the susceptor 220 when the susceptor 220 is heated. A temperature sensor 237 for measuring the temperature of a wafer may also be included if desired.

[0029] An upper clamping ring 248 extends around the periphery of the outer surface of the upper domes 214. A lower clamping ring 250 extends around the periphery of the outer surface of the lower dome 216. The upper and lower clamping rings are secured together so as to clamp the upper and lower domes 214 and 216 to the side wall 218.

[0030] Reactor 210 includes a deposition gas inlet manifold 230 for feeding process gas into chamber 212. Gas inlet manifold 230 includes a connector cap 238, a baffle 274, an insert plate 279 positioned within sidewall 218, and a passage 260 formed between upper liner 282 and lower liner 284. Passage 260 is connected to the upper portion 222 of chamber 212. Process gas from gas cap 238 through baffle 274, insert plate 279 and passage 260 and into the upper portion 222 of chamber 212.

[0031] Reactor 210 also includes an independent inert gas inlet 262 for feeding an inert purge gas, such as but not limited to, Hydrogen (H_2) and Nitrogen (N_2), into

the lower portion 224 of deposition chamber 212. As shown in Figure 2A, inert purge gas inlet 262 can be integrated into gas inlet manifold 230, if desired, as long as a physically separate and distinct passage 262 through baffel 274, insert plate 279, and lower liner 284 is provided for the inert gas, so that the inert purge gas can be controlled and directed independent of the process gas. Inert purge gas inlet 262 need not necessarily be integrated or positioned along with deposition gas inlet manifold 230, and can for example be positioned on reactor 210 at an angle of 90° from deposition gas inlet manifold 230.

[0032] Reactor 210 also includes a gas outlet 232. The gas outlet 232 includes an exhaust passage 290 which extends from the upper chamber portion 222 to the outside diameter of sidewall 218. Exhaust passage 290 includes an upper passage 292 formed between upper liner 282 and lower liner 284 and which extends between the upper chamber portion 222 and the inner diameter of sidewall 218. Additionally, exhaust passage 290 includes an exhaust channel 294 formed within insert plate 279 positioned within sidewall 218. A vacuum source, such as a pump (not shown) for creating low or reduced pressure in chamber 212 is coupled to exhaust channel 294 on the exterior of sidewall 218 by an outlet pipe 233. Thus, process gas fed into the upper chamber portion 222 is exhausted through the upper passage 292, through exhaust channel 294 and into outlet pipe 233.

[0033] The single wafer reactor shown in Figure 2 is a "cold wall" reactor. That is, sidewall 218 and upper and lower liners 282 and 284, respectively, are at a substantially lower temperature than preheat ring 228 and susceptor 220 (and a wafer placed thereon) during processing. For example, in a process to deposit an epitaxial silicon film on a wafer, the susceptor and wafer are heated to a temperature of between 900-1200°C while the sidewall (and liners) are at a temperature of about 400-600°C. The sidewall and liners are at a cooler temperature because they do not receive direct irradiation from lamps 234 due to reflectors 235, and because cooling fluid is circulated through sidewall 218.

[0034] Gas outlet 232 also includes a vent 296 which extends from the lower chamber portion 224 through lower liner 284 to exhaust passage 290. Vent 296 preferably intersects the upper passage 292 of exhaust passage 290 as shown in Figure 2A. Inert purge gas is exhausted from the lower chamber portion 224 through vent 296, through a portion of upper chamber passage 292, through exhaust channel 294, and into outlet pipe 233. Vent 296 allows for the direct exhausting of purge gas from the lower chamber portion to exhaust passage 290.

[0035] According to the present invention, process gas or gases 298 are fed into the upper chamber portion 222 from gas inlet manifold 230. A process gas, according to the present invention, is defined as gas or gas mixture which acts to remove, treat, or deposit a film on a wafer or a substrate placed in chamber 212. According to the present invention process gas comprising HCl and an inert gas, such as H_2, is used to treat a silicon surface by removing and smoothing the silicon surface. In an embodiment of the present invention deposition gas is used to deposit a silicon epitaxial layer on a silicon surface of a wafer placed on susceptor 220 after the silicon surface has been treated. Deposition gas 298 generally includes a silicon source, such as but not limited to, monosilane, trichlorolsilane, dichlorolsilane, and tetrachlorosilane, and a dopant gas source, such as but not limited to phosphine, diborane and arsine. A carrier gas, such as H_2 is generally included in the deposition, gas stream. For an approximately 5 liter chamber, a deposition gas stream between 35-75 SLM (including carrier gas) is typically fed into the upper chamber portion 222 to deposit a layer of silicon on a wafer. The flow of process gas 298 is essentially a laminar flow from inlet passage 260, across preheat ring 228, across susceptor 220 (and wafer), across the opposite side of preheat ring 228, and out exhaust passage 290. The process gas is heated to a deposition or process temperature by preheat ring 228 susceptor 220, and the wafer being processed. In a process to deposit an epitaxial silicon layer on a wafer, the susceptor and preheat ring are heated to a temperature of between 800-1200°C. A silicon epitaxial film can be formed at temperatures as low as 600°C with silane by using a reduced deposition pressure.

[0036] Additionally, while process gas is fed into the upper chamber portion, an inert purge gas or gases 299 are fed independently into the lower chamber portion 224. An inert purge gas is defined as a gas which is substantially unreactive at process temperatures with chamber features and wafers placed in deposition chamber 212. The inert purge gas is heated by preheat ring 228 and susceptor 220 to essentially the same temperature as the process gas while in chamber 212. Inert purge gas 299 is fed into the lower chamber portion 224 at a rate which develops a positive pressure within lower chamber portion 224 with respect to the process gas pressure in the upper chamber portion 222. Process gas 298 is therefore prevented from seeping down through gap 229 and into the lower chamber portion 224, and depositing on the backside of susceptor 220.

[0037] Figure 2B shows a portion of the gas inlet manifold 230 which supplies gas to the upper zone of the processing chamber. In Figure 2B the insert plate 279 is shown to be constituted by a central zone 128 and an outside zone 130. According to this embodiment of the invention the composition of the process gas which flows into the central zone 128 can be controlled independently of the composition of the gas which flows into the outside zones 130. In addition, the flow rate of the gas to either of the two halves 128a - 128b of the central zone can be further controlled independently from one another. This provides two degrees of control for the gas flow for the purposes of controlling the composition of

the process gas mix over different zones of the semiconductor wafer.

[0038] Processing apparatus 210 shown in Figure 2A includes a system controller 150 which controls various operations of apparatus 210 such as controlling gas flows, substrate temperature, and chamber pressure. In a embodiment of the present invention the system controller 150 includes a hard disk drive (memory 152), a floppy disk drive and a processor 154. The processor contains a single board computer (SBC), analog and digital input/output boards, interface boards and stepper motor controller board. Various parts of CVD system 300 conform to the Versa Modular Europeans (VME) standard which defines board, card cage, and connector dimensions and types. The VME standard also defines the bus structure having a 16-bit data bus and 24-bit address bus.

[0039] System controller 150 controls all of the activities of the apparatus 210. The system controller executes system control software, which is a computer program stored in a computer-readable medium such as a memory 152. Preferably, memory 152 is a hard disk drive, but memory 152 may also be other kinds of memory. The computer program includes sets of instructions that dictate the timing, mixture of gases, chamber pressure, chamber temperature, lamp power levels, susceptor position, and other parameters of a particular process. Of course, other computer programs such as one stored on another memory device including, for example, a floppy disk or another appropriate drive, may also be used to operate controller 150. An input/output device 156 such as a CRT monitor and a keyboard is used to interface between a user and controller 150.

[0040] The process for smoothing a silicon surface in accordance with the present invention can be implemented using a computer program product which is stored in memory 152 and is executed by processor 154. The computer program code can be written in any conventional computer readable programming language, such as, 68000 assembly language, C, C + +, Pascal, Fortran, or others. Suitable program code is entered, into a single file, or multiple files, using a conventional text editor, and stored or embodied in a computer usable medium, such as a memory system of the computer. If the entered code text is in a high level language, the code is compiled, and the resultant compiler code is then linked with an object code of precompiled windows library routines. To execute the linked compiled object code, the system user invokes the object code, causing the computer system to load the code in memory, from which the CPU reads and executes the code to perform the tasks identified in the program. Also stored in memory 152 are process parameters such as process gas flow rates (e.g., H_2 and HCl flow rates), process temperatures and process pressure necessary to carry out the smoothing of silicon films in accordance with the present invention.

[0041] Figure 2C illustrates an example of the hierarchy of the system control computer program stored in memory 156. The system control program includes a chamber manager subroutine 170. The chamber manager subroutine 170 also controls execution of various chamber component subroutines which control operation of the chamber components necessary to carry out the selected process set 178. Examples of chamber component subroutines are process gas control subroutine 172, pressure control subroutine 174 and a lamp control subroutine 176. Those having ordinary skill in the art would readily recognize that other chamber control subroutines can be included depending on what processes are desired to be performed in the process chamber 212. In operation, the chamber manager subroutine 170 selectively schedules or calls the process component subroutines in accordance with the particular process set being executed. Typically, the chamber manager subroutine 170 includes steps of monitoring the various chamber components, determining which components needs to be operated based on the process parameters for the process set to be executed and causing execution of a chamber component subroutine responsive to the monitoring and determining steps.

[0042] The process gas control subroutine 172 has program code for controlling process gas composition and flow rates. The process gas control subroutine 172 controls the open/dose position of the safety shut-off valves, and also ramps up/down the mass flow controllers to obtain the desired gas flow rates. The process gas control subroutine 172 is invoked by the chamber manager subroutine 170, as are all chamber component subroutines and receives from the chamber manager subroutine process parameters related to the desired gas flow rates. Typically, the process gas control subroutine 172 operates by opening the gas supply lines, and repeatedly (i) reading the necessary mass-flow controllers 142, (ii) comparing the readings to the desired flow rates received from the chamber manager subroutine 170, and (iii) adjusting the flow rates of the gas supply lines as necessary. Furthermore, the process gas control subroutine 172 includes steps for monitoring the gas flow rates for unsafe rates, and activating the safety shut-off valves when an unsafe condition is detected.

[0043] The pressure control subroutine 176 comprises program code for controlling the pressure in the chamber 212 by regulating the size of the opening of the throttle valve is set to control the chamber pressure to the desired level in relation to the total process gas flow, size of the process chamber, and pumping setpoint pressure for the exhaust system. When the pressure control subroutine 174 operates to measure the pressure in the chamber 212 by reading one or more conventional pressure nanometers connected to the chamber, compare the measure value(s) to the target pressure, obtain PID (proportional, integral, and differential) values from a stored pressure table corresponding to the target pressure, and adjust the throttle valve according to the PID values obtained from the pressure table.

Alternatively, the pressure control subroutine 374 can be written to open or close the throttle valve to a particular opening size to regulate the chamber 212 to the desired pressure.

[0044] The lamp control subroutine 176 comprises program code for controlling the power provided to lamps 234 used to heat the substrate. The lamp control subroutine 176 is also invoked by the chamber manager subroutine 170 and receives a target, or setpoint, temperature parameter. The lamp control subroutine 176 measures the temperature by measuring voltage output of the temperature measurement devices directed at the susceptor 220 compares the measured temperature to the setpoint temperature, and increases or decreases power applied to the lamps to obtain the setpoint temperature.

Process For Treating A Silicon Film

[0045] The present invention describes a method for treating the surface of a silicon or silicon alloy film or substrate. The process of the present invention is ideally suited to teat the surface of a deposited epitaxial silicon film. The silicon surface to be treated however need not necessarily be an epitaxial silicon film and can be for example the surface of a monocrystalline silicon substrate, or can also be the surface of an epitaxial silicon alloy such as an epitaxial silicon germanium (SiGe) alloy. Additionally, the silicon film or substrate to be treated can be doped with impurities such as but not limited to arsenic, phosphorus, and boron or can be undoped if desired. Although amorphous and polycrystalline forms of silicon and silicon alloys typically have very rough surfaces which can not be smoothened to the same degree as monocrystalline films and substrates, the surface treatment of the present invention can still be used to improve the surface roughness of amorphous and polycrystalline silicon and silicon alloy films and to improve the surface quality. The present invention can be used to treat the surface of any silicon or silicon alloy film or substrate requiring some degree of surface smoothing or contamination removal.

[0046] The first step, as set forth in block 102 of flow chart 100 in Fig. 1, to treat a silicon or silicon alloy surface in accordance with the present invention, a substrate having a silicon or silicon alloy surface or film to be treated is placed into a thermal processing chamber such as chamber 222 of apparatus 210 shown in Figure 2A. According to an embodiment of the present invention, the silicon or silicon alloy film to be smoothened is an epitaxial silicon or silicon alloy having a surface roughness of at least 0.2nm RMS and typically at least 0.8 RMS as measured by a Digital Instrument Tapping Mode AFM (Atomic Force Microscopy). RMS is the Root mean square average of the roughness of the surface. The method and apparatus of the present invention can be used to smooth an epitaxial silicon or silicon alloy having a surface roughness of greater than 6nm RMS. In one embodiment of the present invention, substrate 300 is a silicon on insulator (SOI) substrate such as shown in Figure 3A. Silicon on insulator (SOI) substrate 300 includes a monocrystalline silicon substrate 304. An oxide film 306 is on the monocrystalline silicon substrate 304 and an epitaxial film silicon film 302 is on the oxide film 306.

[0047] Next, as set forth in block 104, substrate 300 is heated to a temperature between 1000°- 1300°C and preferably between 1050° - 1200°C Substrate 300 is heated to a temperature which is sufficient to cause silicon atoms to migrate. In this way, silicon atoms which are located at the peaks or high spots of the rough silicon can migrate to the valleys and thereby aid in the smoothing of silicon 302. Substrate 300 can be heated to a temperature between 1000°-1300°C by heating preheat ring 228, susceptor 220 and substrate 300 with radiation from lamps 234.

smooth

[0048] Next, as set forth in block 106 of flow chart 100, a reactant gas mix comprising HCl and an inert gas is fed into chamber 212 as substrate 300 is heated to a temperature between 1000°-1300°C. The inert gas is preferably hydrogen (H_2). Although hydrogen is the preferred inert gas other inert gases such as, but not limited to nitrogen (N_2), helium (He) and argon (Ar) can be used in place of hydrogen. Additionally, although HCl is the preferred etchant gas used for treating a silicon or silicon alloy surface other hydrogen bearing etchants such as but not limited to HBr, HI and HF may be suitable.

[0049] In an embodiment of the present invention H_2 and HCl are fed into the chamber 212 to generate an HCl to H_2 molecular concentration ratio between 1:1000 to 1:100. In a preferred embodiment of the present invention H_2 and HCl are fed into chamber 212 while chamber 212 is maintained at approximately atmospheric pressure, however reduced pressures may be utilized if desired. Heat from susceptor 220, preheat ring 228, and substrate 300 placed on susceptor 220 causes the thermal disassociation of H_2 and HCl which then react with silicon film 302 to remove the top portion thereof. Silicon film 302 can be removed at a rate between 5-80 nm/min.

[0050] The concentration ratio and total gas flow of H_2 and HCl fed into chamber 222 determines the removal rate of silicon 302. Figure 4 illustrates the silicon etch rate (manometers/minute) of various HCl flow rates (SLM) for a constant 90 SLM H_2 flow while substrate 300 is heated to a temperature of 1100°C. As is readily apparent from the graph of Figure 4, as the HCl:H_2 concentration ratio increases the removal rate increases. It is to be noted that the ability of the present invention to smooth a silicon surface is dependent upon the amount of time the substrate is held at an elevated temperature. That is, since high removal rates use shorter times of etching, the smoothing is not as good. However, if one removes silicon for a long period of time, for example greater than 3 minutes, then both low and high removal rates can generate smooth silicon surfaces. Thus, high

removal rates can be used to provide a smooth silicon surface as long as the substrate is exposed to reactants and to high temperatures for a sufficiently long period of time. In an embodiment of the present invention where, for example more than 100nm of silicon film 302 is to be removed, first a high $HCl:H_2$ concentration ratio is used to provide a high removal rate to remove the bulk of the silicon film, and then a low $HCl:H_2$ concentration ratio is used to reduce the removal rate towards the end of the treatment process.

[0051] H_2 and HCl is continually fed into chamber 222 until a sufficiently smooth top surface 303 of silicon film 302 is obtained. In an embodiment of the present invention H_2 and HCl are fed into chamber 222 until the top surface of silicon film 302 obtains an RMS value of less than 0.5nm and preferably less than 0.1nm, as shown in Figure 3B. In an embodiment of the present invention, film 302 is treated with H2 and HCl at a temperature between 1000° -1300°C until less then approximately 100Å of silicon film 302 remains. It is to be appreciated that the outstanding uniformity of the treatment process of the present invention enables thin films of less than 100Å to be formed across the surface of a wafer by a subtractive or removal process. Other removal processes, such as polishing, which do not have the removal uniformity of the present invention can not reliably produce such thin films across the surface of a wafer or substrate.

[0052] It has been found that in apparatus 210 the removal rate of a silicon film located at the center of chamber 212 is different then the removal rate of the silicon film located at the outer section of chamber 212. As such, in an embodiment of the present invention the gas flow of HCl/H_2 is controlled so that the outer section 130 of the upper chamber portion 222 receives one HCl/H_2 gas flow while the inner section 128 of the upper chamber portion 222 receives a second different HCl/H_2 gas flow. In one embodiment of the present invention the inner section 128 of chamber 212 receives a higher gas flow of HCl/H_2 than does the outer section 130. In another embodiment of the present invention the inner section 128 of chamber 212 receives a lower gas flow of HCl/H_2 than does the outer section 130.

[0053] Next, if desired, as set forth in block 108 a flow chart 100, a silicon film 308 is deposited onto the smooth surface 303 of silicon film 302 as shown in Figure 3C. In one embodiment of the present invention a silicon epitaxial film is deposited over the HCl/H_2 exposed silicon film 302. Because the surface of silicon film 302 is smooth and uniform a silicon, film 308 having a smooth surface can be formed over silicon film 302. In one embodiment of the present invention, an epitaxial silicon film 308 is deposited onto silicon film 302 in the same chamber (e.g., chamber 212) in which the surface of the silicon film *was* made smooth. In this way, a silicon film 308 can be formed directly onto the smooth surface of silicon film 302 without removing substrate 300 from chamber 212 and exposing silicon film 302 to an oxidizing ambient (e.g. air) or to other potential contaminants.

[0054] The deposited silicon film 308 can be doped or undoped and preferably is epitaxial silicon. Deposited silicon film 308 however can be amorphous or polycrystalline silicon or a silicon alloy such as silicon germanium. Depositing silicon film 308 onto silicon film 302 enables the formation of a smooth silicon film having any thickness and any dopant density required. By adding an additional silicon layer 308 after the silicon surface treatment process, more silicon can be removed during the treatment process in order to ensure a suitable surface finish without having to preserve silicon to ensure that a sufficient amount of silicon is available for the formation of devices.

[0055] In one embodiment of the present invention a silicon epitaxial film 308 is formed onto the smooth surface 303 of film 302. A silicon epitaxial film 308 can be formed by heating substrate 300 to a temperature between 800-1200°C and flowing a deposition gas comprising a silicon source gas such as but not limited to silane, dichlorosilane, trichlorosilane, etc. and H_2 into chamber 212. If a doped silicon film 308 is desired then a n-type dopant, such as phosphine or arsine, or a p-type dopant such as diborane can be included in the gas mix to obtain any dopant conductivity type and density as desired for silicon film 308.

[0056] Figures 6A-6I illustrate an embodiment of the present invention where the HCl treatment process of the present invention is used to provide a surface finishing of a silicon film roughened by an implant and cleave process. As illustrated in Figure 6A-6I the implant and cleave process can be used to form a silicon on insulator (SOI) substrate. Figure 5 is an example of a cluster tool 500 in which the formation of a silicon on insulator substrate in accordance with the present invention can be formed. Cluster tool 500 includes a transfer chamber 502 to which are attached a plurality of different process apparatuses including, an implant chamber 504, a bond/cleave chamber 506, a surface Treatment/Epi chamber 508, such as apparatus 210 shown in Figure 2A, an oxide formation apparatus 510 and a loadlock 512. Other chambers, such as a cool down chamber or chambers and/or additional loadlocks, can be attached to transfer chamber 502 as required.

[0057] Implant chamber 504 is used to implant ions into a donor wafer to form dislocations in the donor substrate to enable the subsequent cleave of the silicon film. Bond/cleave apparatus 506 is used to bond the handle wafer to the implanted donor wafer and is used to cleave the donor wafer from the handle wafer at the implant dislocation. The Treatment/Epi chamber 508 is used to treat or smooth the surface of the silicon film after the cleave process and can be used to deposit an epitaxial silicon film on the treated silicon surface. The Treatment/Epi apparatus can also be used to smooth the silicon surface of the donor wafer and to deposit additional silicon thereon if desired. Loadlock 510 is used to transfer wafers or substrates into a transfer chamber 502 of

cluster tool 500. Transfer chamber 502 is attached to an exhaust system such as a pump and a source of inert gas, such as nitrogen (N_2) so that wafers can be transferred between the various process apparatuses in cluster tool 500 in a reduced pressure ambient or in an inert ambient so that wafers are not exposed to an oxidizing ambient or to sources of contamination. Oxide formation apparatus 510 is used to form an oxide on the donor wafer (or handle water if desired). Oxide formation apparatus can be for example, a thermal oxidation apparatus such as a fumace or a rapid thermal processor in which a thermal oxide can be grown on a silicon film. Altematively, oxide formation apparatus 510 can be a chemical vapor deposition (CVD) apparatus.

[0058] In order to form a silicon on insulator (SOI) substrate in accordance with an embodiment of the present invention, a handle wafer 600 and a donor wafer 650 as shown in Figure 6A are provided. The donor wafer 650 is the wafer (or substrate) which provides a layer or layers to be transferred. The handle wafer 600 is the wafer which receives the transferred layers from the donor wafer and is the wafer which will eventually become the silicon on insulator (SOI) substrate. Handle wafer 600 includes a monocrystalline silicon substrate 602. Silicon substrate 602 can be doped to any conductivity type (n-type or p-type) and to any conductivity level desired. In one embodiment of the present invention silicon substrate 600 is a p-type substrate having a doping density of between 10^{15} - 10^{19} atoms/cm^3. Handle wafer 600 can also include an oxide film 604 formed thereon. In an embodiment of the present invendon Oxide film 604 is between 100 - 400nm thick. Oxide film 604 can be thermally grown by exposing silicon substrate 602 to an oxidizing ambient, such as oxygen, at a temperature between 800-1250°C in apparatus 510.

[0059] Donor wafer 650 includes a monocrystalline silicon substrate 652 with an oxide film 654 formed thereon. Silicon substrate 650 can be doped to any desired conductivity type and level desired. In an embodiment of the present invention silicon substrate can be doped to a level between 10^{15} - 10^{19} atoms/cm^3. Oxide film 654 can be formed by thermal layer oxidizing silicon substrate 650 in an oxidizing ambient in apparatus 510 as described above. Oxide film 654 typically has a thickness between 100-400nm. Alternatively, to growing an oxide on both donor wafer 650 and handle wafer 600 one can grow an oxide on only donor wafer 650 or on only handle wafer 600 if desired.

[0060] Next, as shown is Figure 6B, donor wafer 650 is moved into implant chamber 504 and is implanted with ions to form dislocation 656. Donor wafer 650 can be implanted with hydrogen atoms or with inert ions such argon (AT) or helium (He). In one embodiment of the present invention substrate 650 is ion implanted with a plasma immersion ion implantation process. Such a process can implant high doses of hydrogen H_2 into substrate 652. In such a process a high voltage negative bias is applied to donor wafer 650 to accelerate the ions towards the wafer face (oxide layer 654). The plasma immersion ion implantation process implants the entire donor wafer surface. The P-III Ion Implantation System developed by Silicon Genesis can be used for a plasma immersion ion implantation step. Additionally, ion implantation can be carried out using for example beam line ion implantation equipment manufactured from companies such as Applied Materials, Eaton Corp. Varian and others. The implantation of hydrogen generates an intemal hydrogen rich layer 656 within the donor wafer 650. The depth, D, of the ion implantation peak determines the amount of silicon 658 which will subsequently be removed from silicon substrate 652 of donor wafer 650. In an embodiment of the present inventions ions are implanted between 100-500nm into substrate 652 of donor wafer 650.

[0061] Next, the ion implanted donor wafer 650 and the handle wafer 600 are placed into bond/cleave apparatus 506. In bond/cleave apparatus 506 donor wafer 650 is bonded to handle wafer 600 as shown in Figure 6D. In one embodiment of the present invention oxide 654 of donor wafer 650 is bonded to oxide 604 of handle wafer 600. In an embodiment of the present invention the handle and donor wafers are bonded using a low temperature plasma activated bond process. By using plasma activation of the bond interface, higher bond strength can be achieved at low process temperatures (e.g. room temperature). In accordance with an embodiment of the present invention both the handle wafer and the donor wafer are exposed to a low temperature plasma as shown in Figure 6C in order to generate plasma activated bonding surfaces 606 and 660 respectably. It is to be appreciated that other suitable bonding techniques may be used to bond the handle wafer to the donor wafer.

[0062] Next, the donor wafer 650 is flipped upsidedown so that bond interface 660 can be attached to the bond interface 606 of handle wafer 600 as shown in Figure 6D. The donor and handle wafer stack is then compressed together to securely bond interface 662 interface 606. Plasma activation of the bond interface helps achieve a sufficiently strong bonding for a subsequent room temperature cleave process.

[0063] Next, as shown in Figure 6E, the lower portion 659 of silicon substrate 652 is separated or cleaved from upper portion of silicon layer 658 at dislocation 656 of donor wafer 650. In an embodiment of the present invention a Room Temperature Controlled Cleaved Process (RT/CCP) is used to separate the bonded pair at the implant dislocation 656 without using heat The RT/CCP process initiates a separation at one point on the wafer and propogates that separation cross the entire wafer through mechanical means. In one embodiment of the present invention as shown in Figure 6E a nitrogen stream is focused at the edge of the dislocation to cause separation.

[0064] The implant, bond, and leave process transfers oxide film 654 and silicon film 658 to handle wafer

600. The transfer generates a silicon on insulator (SOI) substrate a wafer comprising a silicon wafer (602) with an oxide layer (654/604) buried under a thin layer 658 of monocrystalline silicon. The thickness of the top silicon layer 658 is determined by the depth of the hydrogen implant.

[0065] As shown in Figure 6E, the implant and cleave process forms a very rough silicon surface 660. where *silicon* film 658 is separated from silicon substrate 652. The implant and cleave process will typically form a silicon surface having a surface roughness of between 2-8nm rms. In order to provide a suitable finish, handle wafer 600 along with oxide 654 and silicon 658 is transferred into Treatment/Epi chamber 508 and processed as defined in flow chart 100 of Figure 1 in order to surface treat the rough silicon surface 660 of silicon film 658 into a suitably smooth surface 664 as shown in Figure 6F. Silicon film 658 can be suitably treated by heating handle wafer 600 to a temperature between 1000°C-1300°C and preferably between 1050°C-1200°C and then exposing silicon film 658 to a gas mix comprising H_2 and HCl. In an embodiment of the present invention handle wafer 600 is exposed to a gas mix comprising an $HCl:H_2$ molecular concentration ratio between 1:100 to 1:1000. Handle wafer 600 is heated and exposed to H_2 and HCl until a suitably smooth surface finish 664 of a surface roughness less than 0.5nm RMS and preferably less than 0.1nm RMS is obtained. In an embodiment of the present invention between 50-100mn of silicon film 658 is removed in order to generate a sufficiently smooth surface. In one embodiment of the present invention after silicon film 658 has been sufficiently treated, between 90-300nm of silicon film 658 remains. In another embodiment of the present invention, the top silicon film 658 is treated to thin the film 658 to less than 200Å and preferably between 50-100Å, Such a thin silicon film 658 can be used to produce a compliant substrate for depositing a relaxed defect free epitaxial silicon germanium film.

[0066] Additionally, as described above, the $HCl:H_2$ concentration ratio can be varied during smoothing in order to increase or decrease the removal rate and the $HCl:H_2$ flow can be varied across the surface of the wafer (inner and outer locations) in order to manipulate the removal rate across the surface of the wafer.

[0067] Not only does the smoothing process of the present invention smooth the surface of silicon film 658 but it also repairs damage and removes contamination caused by the implant/ cleave process. For example, the surface treatment process removes hydrogen rich silicon from the surface of silicon film 658. Additionally, the high temperature process used to treat the silicon film repairs dangling silicon bonds created by the implant and leave process. Thus, the high temperature treatment process of the present invention alleviates the need for a subsequent high temperature anneal typically used after cleaving.

[0068] Next, if desired, as shown in Figure 6G a silicon film 666 can be formed on smoothened surface 664 of transferred silicon film 658 if desired. In an embodiment of the present invention a silicon film 666 is formed in the same chamber (e.g. chamber 508) in which silicon film 658 was treated. In this way, treated silicon 658 is not exposed to an oxidizing ambient or to other potential contaminants prior to the formation of silicon film 666.

[0069] In an embodiment of the present invention silicon film 666 is a single crystalline silicon film (epitaxial silicon) formed by chemical vapor deposition using a silicon source gas, such as trichlorosilane or silane and hydrogen gas H_2 Silicon film 666 can be formed to any thickness desired and can be formed to any conductivity type and density desired. In an embodiment of the present invention a silicon film 666 having p-type conductivity type and a dopant density between 10^{15} -10^{19} atoms/cm^3 is formed to a total thickness between 1000Å- 5µm. The ability to do a subtractive and additive process described above in a single chamber can be used to provide a silicon film with any surface finish, thickness, and doping density desired. Alternatively, silicon film 666 can be a silicon alloy such as silicon germanium.

[0070] Additionally, if desired, donor wafer 650 can be placed into Treatment/Epi chamber 508 to treat the surface of silicon film 652 and thereby form a smooth contaminant free surface 668 as shown in Figure 6H. Additionally, if desired additional silicon 670, such as epitaxial silicon, can be deposited onto surface 668 of donor wafer 650 while donor wafer remains in the treatment/ Epi chamber 508 as shown in Figure 6I. In this way, additional silicon can be continually added to the donor wafer after each transfer process thereby enabling the regeneration of the silicon film on the donor wafer and enabling a much longer lifetime of the donor. Additionally, grow an epitaxial silicon film on the donor wafer allows one to precisely control the dopant type and density of silicon on the donor wafer. Alternatively, a silicon alloy such as silicon germanium can be grown on the surface 668 of donor wafer 650.

[0071] Thus, a method and apparatus for treating a silicon or silicon alloy surface has been described. Although the present invention has been described with respect to the treatment of a silicon film of a SOI substrate, and more particularly to a silicon film of a SOI substrate formed by an implant and cleave process, the present invention is not to be limited to these specific embodiments. One skilled in the art will appreciate the ability to use the present invention to treat any silicon a silicon alloy surface where a smooth and contaminant surface is desired.

[0072] Thus, a method and apparatus for treating a silicon surface in order to produce a silicon film with a smooth and contaminant free surface has been described.

Claims

1. A method of treating silicon or silicon alloy surface of a substrate, said method comprising the steps of:

   heating a substrate having a silicon or silicon alloy surface in a chamber to a temperature of between 1000° - 1300°C; and
   exposing said first silicon or silicon alloy surface to a first gas comprising HCl in said chamber while heating said substrate.

2. The method of claim 1 wherein said temperature is between 1050°-1200°C.

3. The method of claim 1 further comprising the step of:
   after exposing said silicon or silicon alloy surface to said first gas mix, depositing in said chamber a silicon film on said silicon surface of said substrate.

4. The method of claim 1 wherein said silicon or silicon alloy surface has a surface roughness of at least 0.2nm RMS prior to exposing said substrate to said first gas.

5. The method of claim 4 wherein said substrate is exposed to HCl until said silicon or silicon alloy has a surface roughness of less than 0.1nm.

6. The method of claim 1 wherein said first gas further comprises H_2.

7. The method of claim 1 wherein the pressure within said chamber while exposing said substrate to said first gas is atmospheric pressure.

8. The method of claim 6 wherein the said first gas has a molecular concentration ratio of HCl to H_2 of between 1:100 to 1:1000.

9. The method of claim 6 further comprising the steps of after exposing said silicon or silicon alloy surface to said first gas exposing said silicon surface to a second gas mix comprising HCl and H_2 while heating said substrate.

10. The method of claim 9 wherein said second gas mix has a different molecular concentration ratio of HCl to H_2 than said first gas.

11. The method of claim 1 wherein said silicon or silicon alloy surface is a silicon or silicon alloy film formed on an oxide film formed on a single crystalline silicon substrate.

12. A method of treating a silicon or silicon alloy surface formed on a substrate, said method comprising the steps of:

   heating a substrate having a silicon surface in a chamber to a temperature of between 1000° -1300°C;
   exposing said silicon or silicon alloy surface to a gas mix comprising H_2 and HCl in said chamber while heating said substrate; and
   depositing in said chamber a silicon film onto said H_2 and HCl exposed silicon or silicon alloy surface.

13. A method of treating a silicon or silicon alloy surface on a substrate, said method comprising the steps of:

   heating a substrate having a silicon surface in a chamber to a temperature of between 1000° -1300°C;
   exposing said silicon or silicon alloy surface to a first gas mix comprising HCl and H_2 while heating said substrate, wherein said first gas mix has a first molecular concentration ratio of HCl and H_2; and
   exposing said silicon or silicon alloy surface to a second gas mix comprising HCl and H_2 while heating said substrate, wherein said second gas mix has a lower molecular concentration ratio of HCl and H_2 then said first gas mix.

14. A method of treating the surface of a silicon or silicon alloy film of a silicon on insulator substrate, said method comprising the steps of:

   heating said substrate in a chamber to a temperature between 1050°C - 1200°C;
   exposing said silicon film to a first gas mix comprising HCl and H_2 in said chamber while heating said substrate, wherein said first gas mix has a molecular concentration ratio of HCl to H_2 between 1:100 to 1:1000;
   exposing said silicon film to a second gas mix comprising HCl and H_2 in said chamber while heating said substrate, wherein said second gas mix has a molecular concentration ratio of HCl:H_2 between 1:100 to 1:1000 and wherein said second gas mix has a molecular concentration ratio of HCl:H_2 which is lower than the molecular concentration ratio of HCl:H_2 of said first gas mix; and
   after exposing said silicon film to said second gas mix, depositing in said Chamber a second silicon film on said silicon film of said silicon on insulator substrate.

15. A substrate processing system comprising:

a substrate holder, located within the chamber, that holds a substrate having a silicon or silicon alloy surface during substrate processing;
a gas delivery system for introducing a process gas mix into said chamber;
a heat source for heating said substrate;
a controller for controlling said gas delivery system and said heat source;
a memory coupled to said controller comprising a computer readable medium having a computer readable program and body therein for directing operation of said substrate processing system, said computer readable program comprising;
instructions for controlling said heat source to heat said substrate to a temperature of between 1000°-1300°C, and instructions for controlling said gas delivery systems to introduce a process gas including HCl while heating said substrate to a temperature of between 1000°-1300°C.

16. A method for treating a film of material, said method comprising:

providing a substrate comprising a cleaved surface, said cleaved surface being characterized by a predetermined surface roughness value and having a distribution of hydrogen bearing particles defined from said cleaved surface to a region underlying said cleaved film; and
increasing a temperature of said cleaved surface to greater than about 1,000 Degrees Celsius while maintaining said cleaved surface in a hydrogen bearing etchant gas to reduce said predetermined surface roughness value by about fifty percent and greater.

17. The method of claim 16 wherein said hydrogen bearing etchant gas is derived from an HCl gas and a hydrogen gas.

18. The method of claim 17 wherein said HCl gas and said hydrogen gas is at a ratio of about 0.001 to 10.

19. The method of claim 18 wherein said ratio of said HCl gas and said hydrogen gas is about 0.001 to 10 and greater.

20. The method of claim 16 wherein said substrate is maintained at about 1 atmosphere during said hydrogen treatment.

21. The method of claim 16 wherein said cleaved surface is provided by a controlled cleave process.

22. The method of claim 16 wherein said substrate is a silicon wafer.

FIG. 1

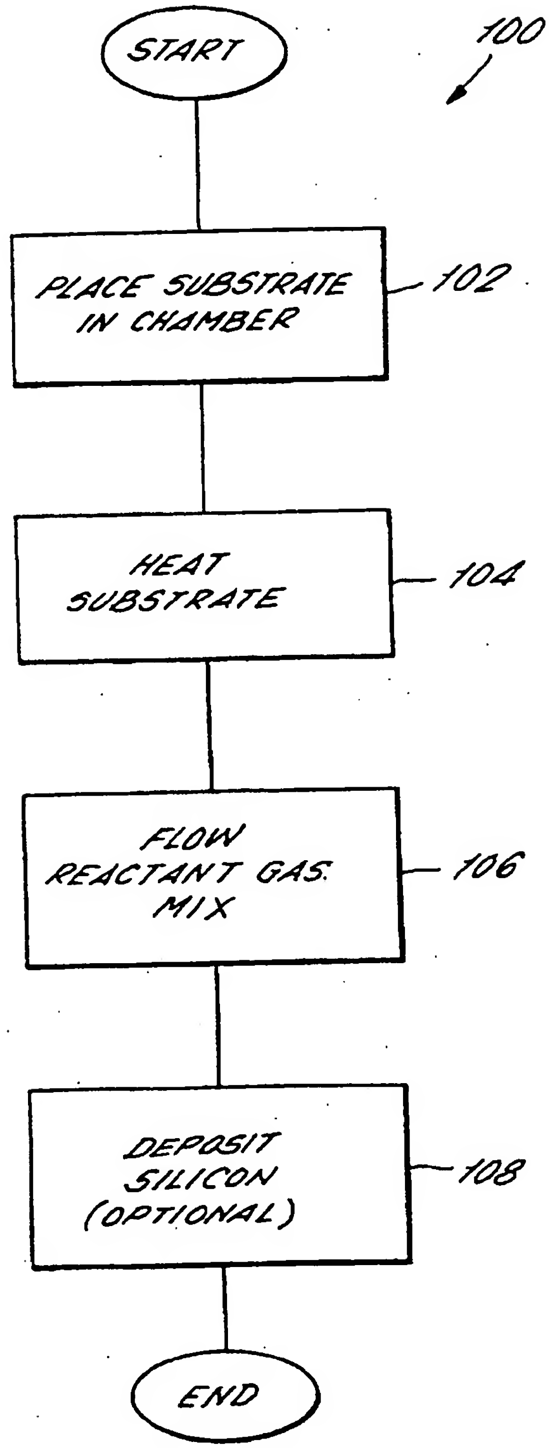
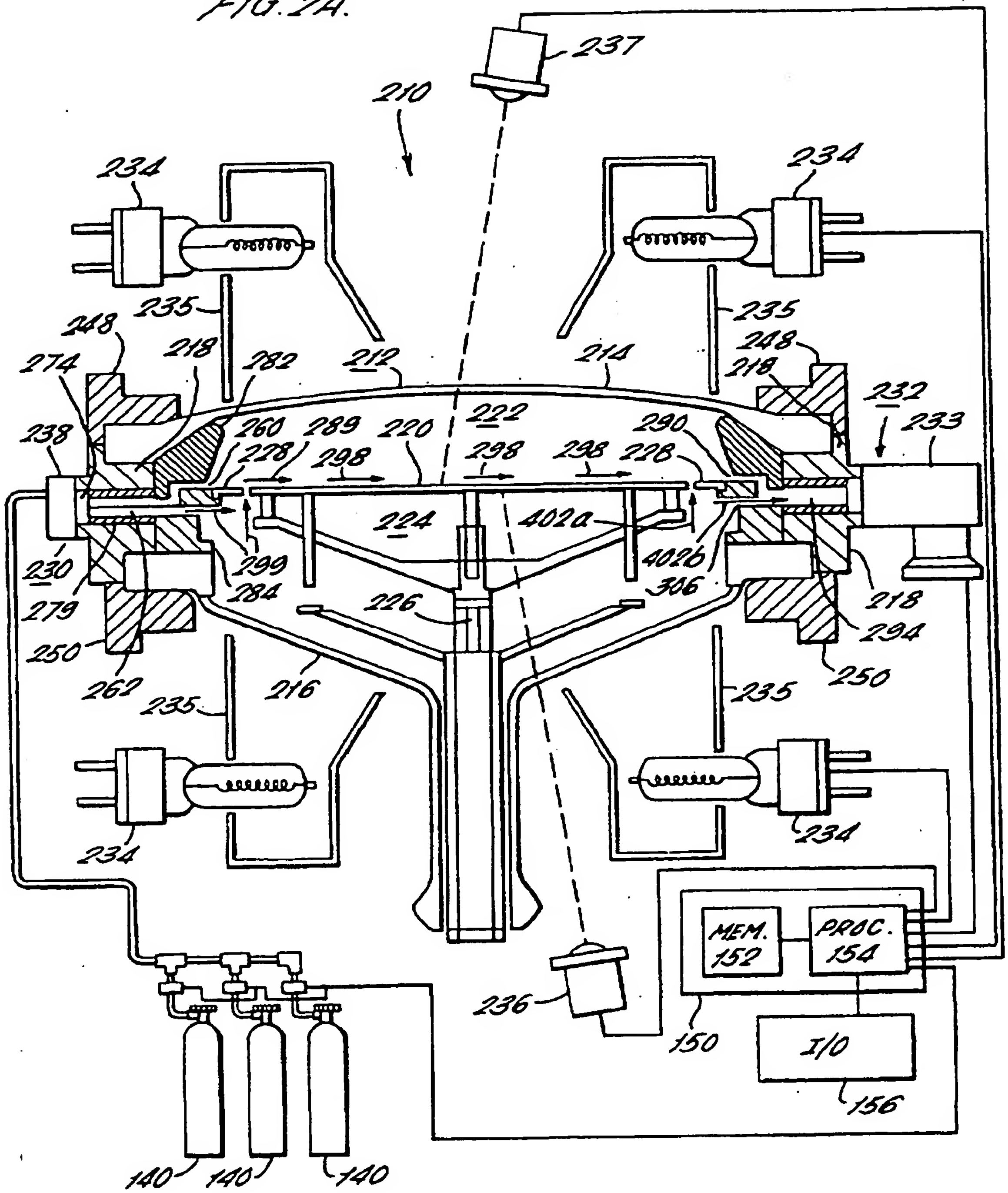

START
PLACE SUBSTRATE IN CHAMBER
102
HEAT SUBSTRATE
104
FLOW REACTANT GAS MIX
106
DEPOSIT SILICON (OPTIONAL)
108
END
100

FIG. 2A.


237
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290
228
298
298
298
228
224
402a
402b
230
299
279
284
306
218
226
294
250
250
262
235
216
235
234
234
MEM. 152
PROC. 154
236
150
I/O
156
140
140
140

FIG. 2B.

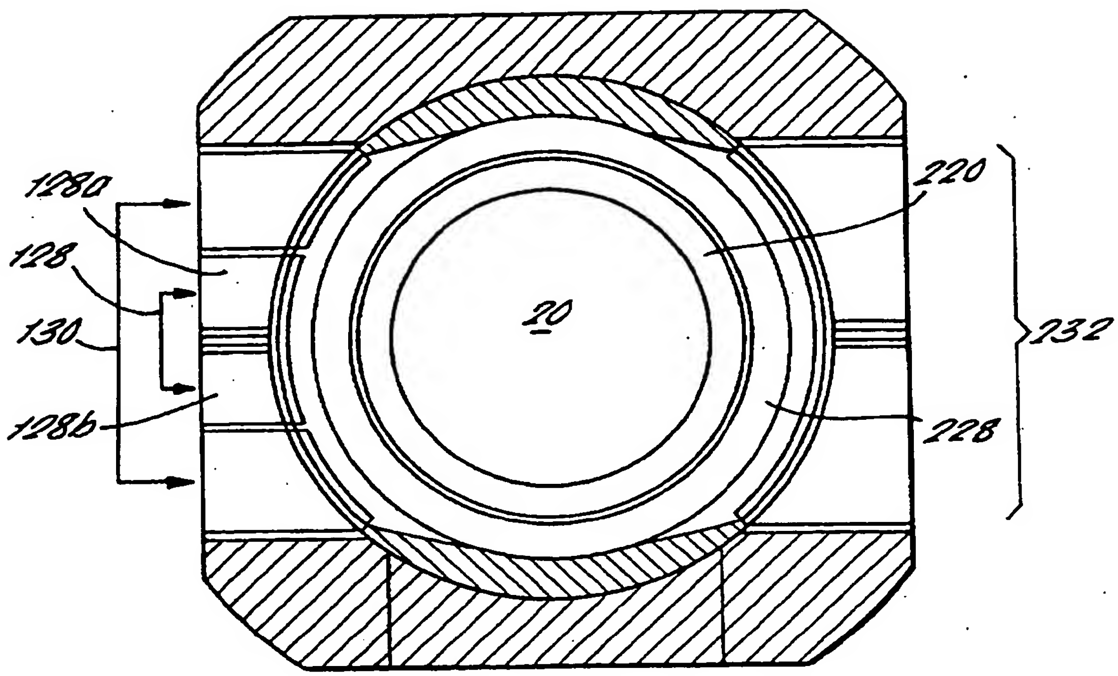

FIG. 2C.

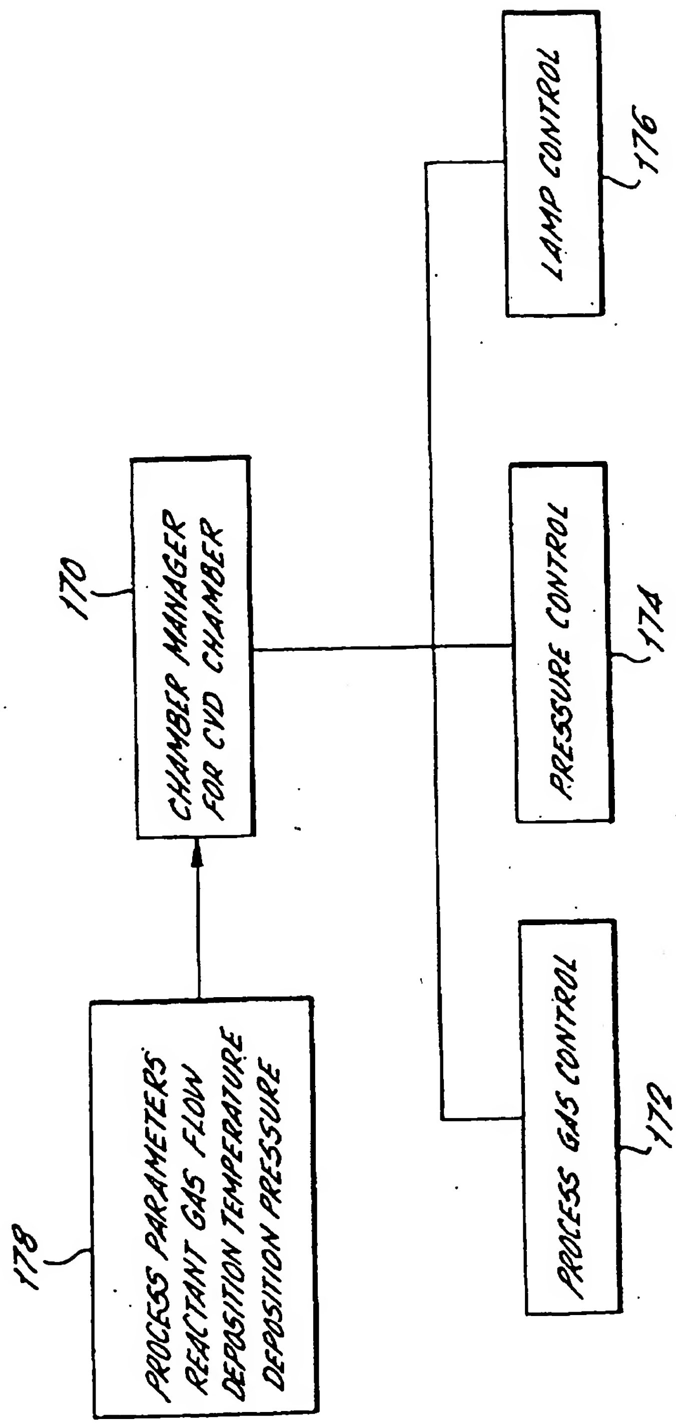
PROCESS PARAMETERS
REACTANT GAS FLOW
DEPOSITION TEMPERATURE
DEPOSITION PRESSURE
178
CHAMBER MANAGER FOR CVD CHAMBER
170
PROCESS GAS CONTROL
172
PRESSURE CONTROL
174
LAMP CONTROL
176

FIG. 3A.

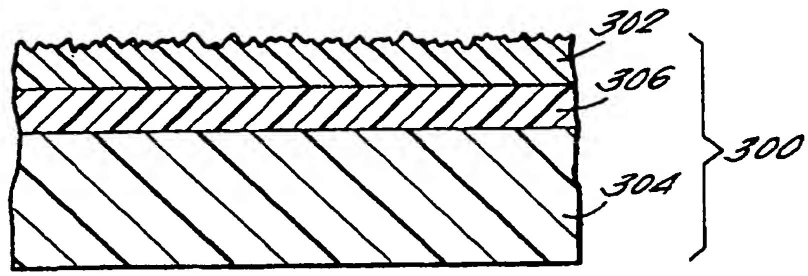

FIG. 3B.

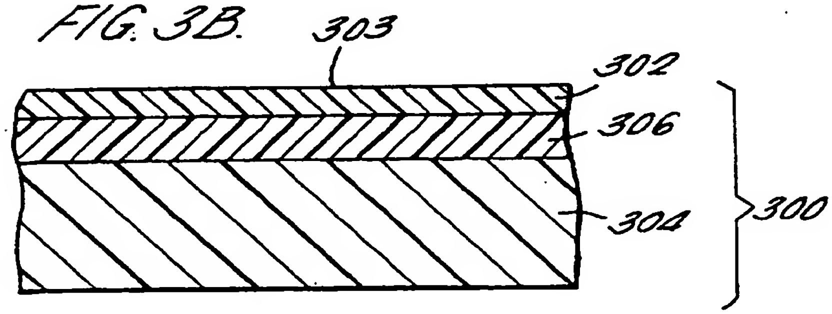

FIG. 3C.

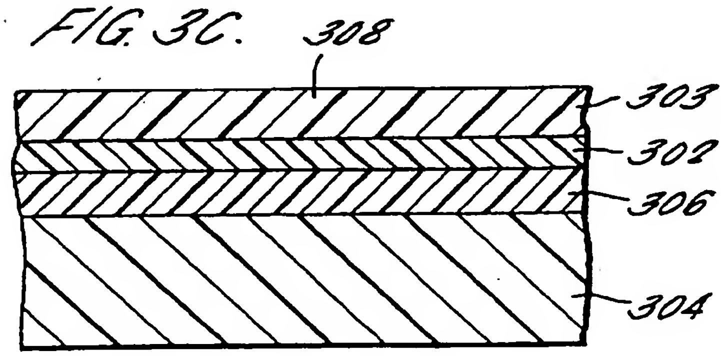

FIG. 4.

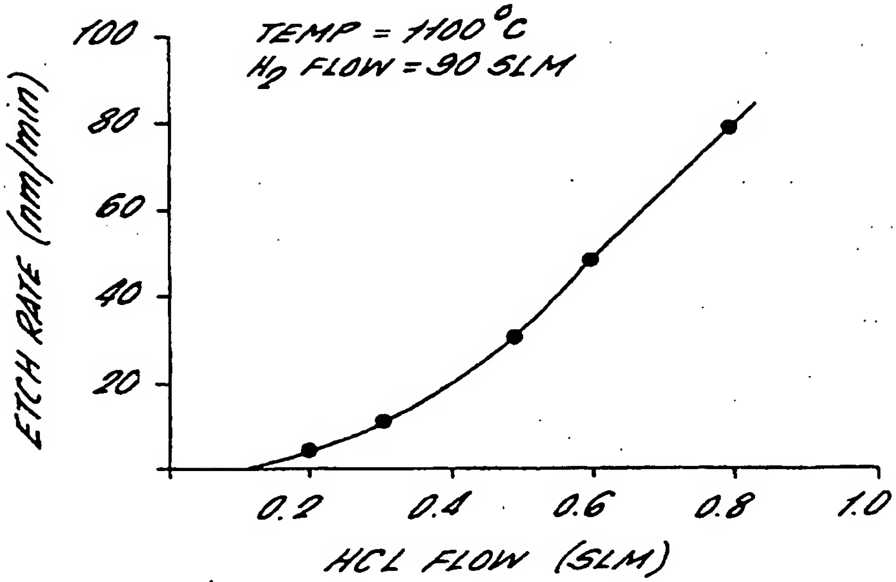
TEMP = 1100°C
H_2 FLOW = 90 SLM
ETCH RATE (nm/min)
100
80
60
40
20
0.2
0.4
0.6
0.8
1.0
HCL FLOW (SLM)

FIG. 5.

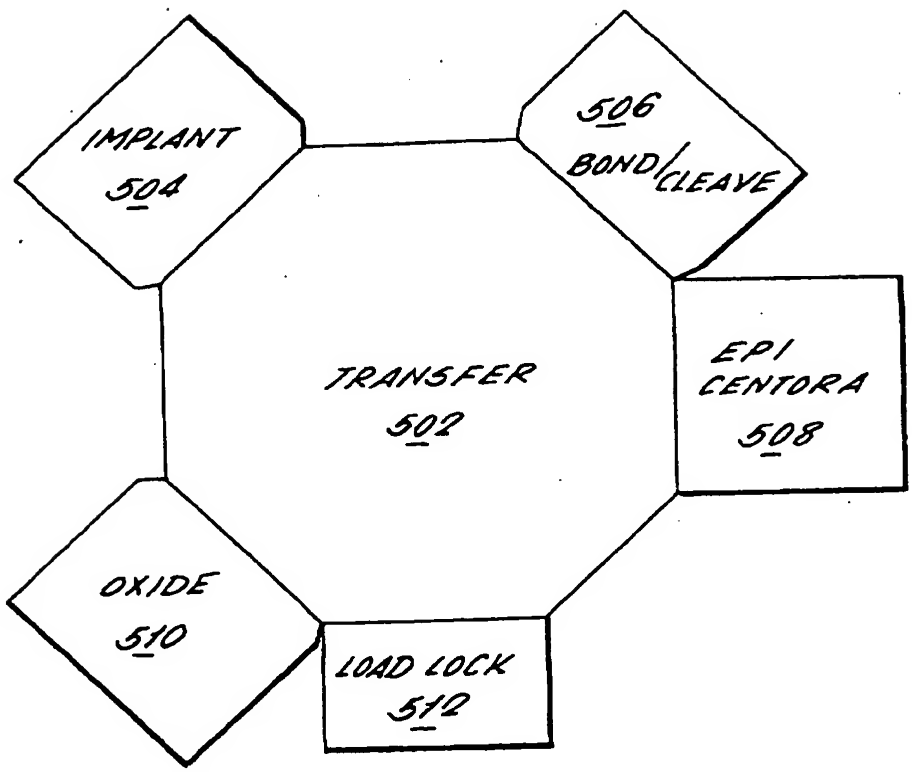
IMPLANT
504
506
BOND/CLEAVE
TRANSFER
502
EPI
CENTORA
508
OXIDE
510
LOAD LOCK
512

FIG. 6A.

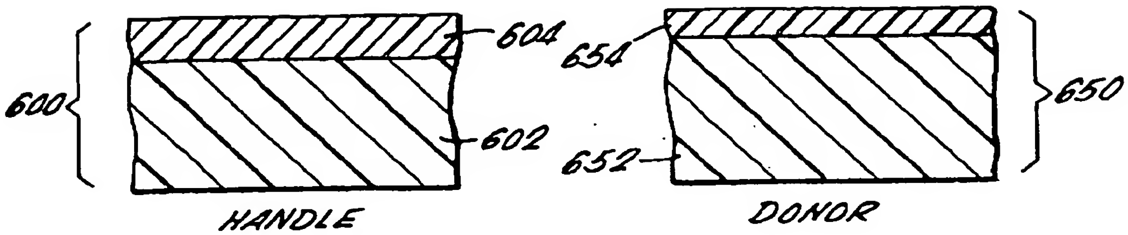

FIG. 6B.

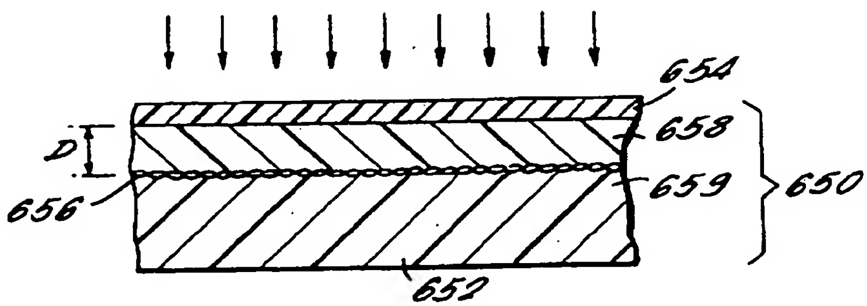

FIG. 6C.

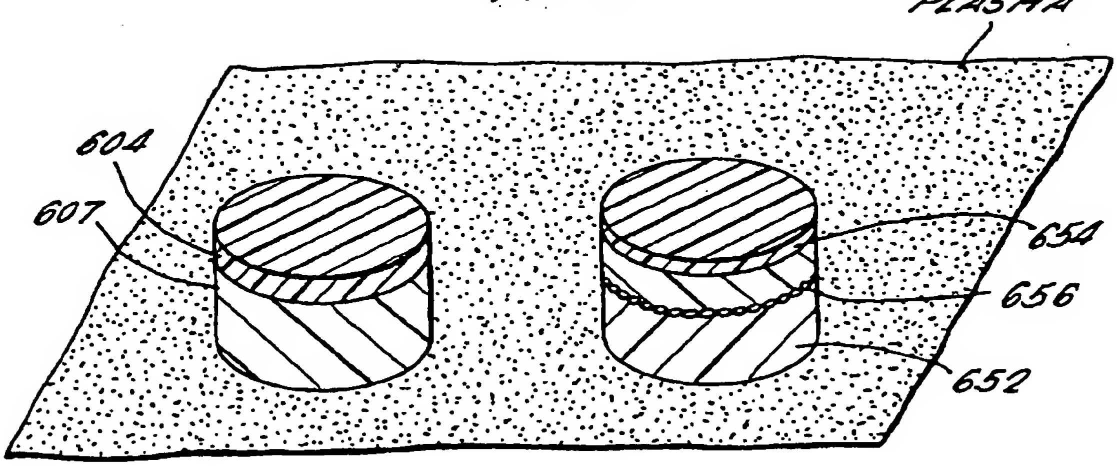

FIG. 6D.

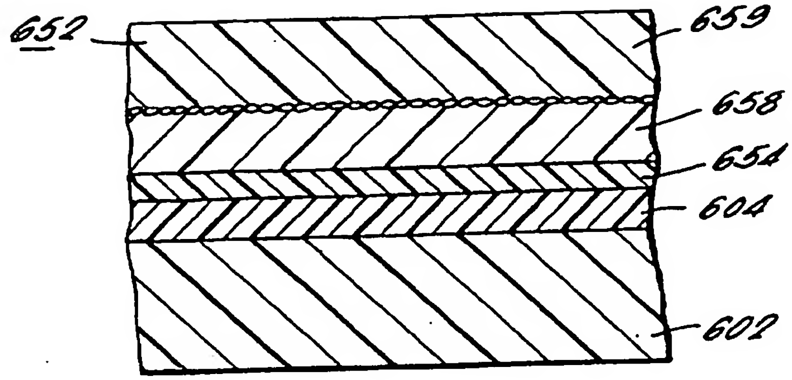

FIG. 6E.

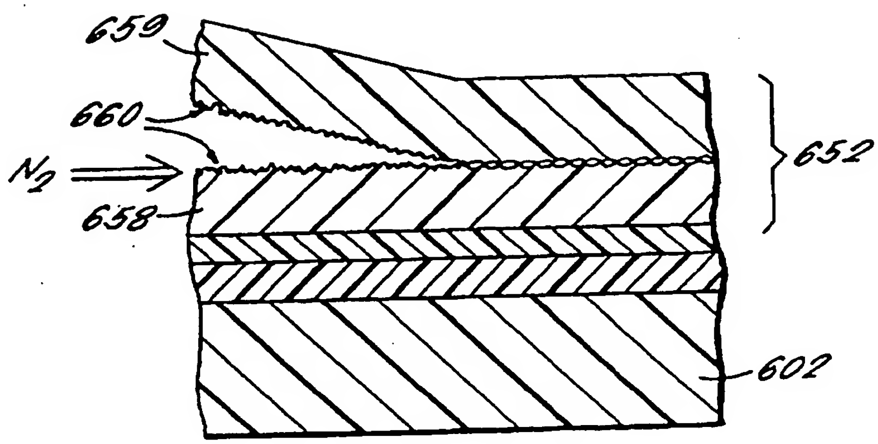

FIG. 6F.

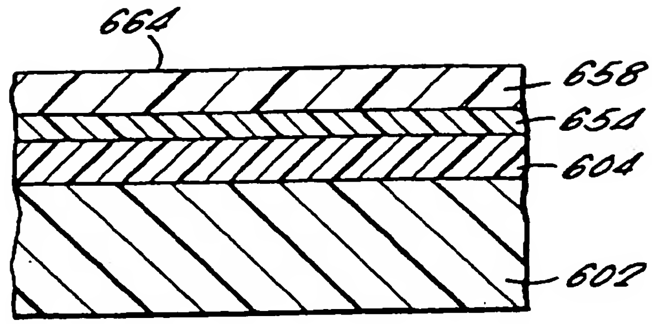

FIG. 6G.

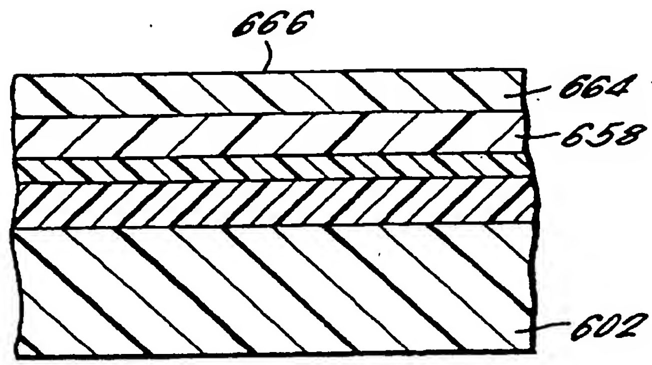

FIG. 6H.

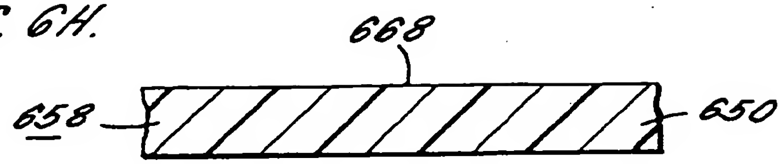

FIG. 6I.